7384-US-A 12F038US

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I declare:

My post office address, residence address and country of citizenship as stated below next to my name are true and correct;

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled "METHOD AND APPARATUS FOR FAULT SIMULATION OF SEMICONDUCTOR INTEGRATED CIRCUIT"
by Masahiro Ishida, Takahiro Yamaguchi and Yoshihiro Hashimoto, described in the patent application filed herewith;

I have reviewed and understand the contents of the above identified application, including the description, claims and drawings, including any amendments specifically referred to herein; and

I acknowledge the duty to disclose information, including information which became available between the filing date of any prior-filed patent applications upon which priority is claimed and the filing date of this application, known to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

I claim benefit of priority under 35 U.S.C. § 119(a)-(d) or § 365(b) for application number 14962/00 filed January 24, 2000 in Japan.

I declare that no foreign application for patent or inventor's certificate and no international patent application has been filed on the same subject matter prior to the earliest-filed application upon which priority is claimed.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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October 10, 2000
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橋本好弘 ____________________ October 10, 2000
Signature (exactly as typed above) Date
Yoshihiro Hashimoto

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POWER OF ATTORNEY

I am an official empowered to act on behalf of ADVANTEST CORPORATION, a corporation of Japan, having a place of business at 32-1, Asahicho 1-chome, Nerima-ku, Tokyo, Japan ("COMPANY").

COMPANY holds all rights, title and interest in the subject matter which is claimed and for which a patent is sought on the invention entitled "METHOD AND APPARATUS FOR FAULT SIMULATION OF SEMICONDUCTOR INTEGRATED CIRCUIT" by Masahiro Ishida, Takahiro Yamaguchi and Yoshihiro Hashimoto, described in the patent application filed herewith, by virtue of assignments from the inventors identified above, for which a copy is attached hereto.

All prior-filed powers of attorney, if any, in connection with this application are hereby revoked and the following are appointed as principal attorneys and agents with full power of substitution and revocation, to appoint other principal and associate attorneys, to prosecute this application, to transact all business in the United States Patent and Trademark Office connected therewith and to receive the original Letters Patent:

Thomas A. Gallagher (Reg. No. 24,815)
David N. Lathrop (Reg. No. 34,655)
Timothy J. Lane (Reg. No. 41,927)

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For Advantest Corporation:

(Signature)

October 10, 2000
(Date)

Hiroshige Ohno
(Printed Name)

Manager of Intellectual Property Dept.
(Title)

Docket: KPO089